Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A wiring substrate in which a bump of an electronic parts is bonded to a connection pad of the wiring substrate, which has a structure in which a wiring pattern including the connection pad is provided on an insulating film, by an ultrasonic flip-chip packaging,
wherein a via hole into which a via post acting as a strut to support the connection pad upon the ultrasonic flip-chip packaging is filled is arranged in the insulating film under the connection pad.

[c2] 2. A wiring substrate in which a bump of an electronic parts is bonded to a connection pad of the wiring substrate, which has a structure in which a wiring pattern including the connection pad is provided on an insulating film, by an ultrasonic flip-chip packaging,
wherein a via hole into which a via post acting as a strut to support the connection pad upon the ultrasonic flip-chip packaging is filled is arranged in a predetermined portion of the insulating film under the wiring pattern connected to the connection pad within 200 μm from the connection pad.

[c3] 3. A wiring substrate according to claim 1 or 2, wherein

the via hole is a dummy via hole and a normal via hole is arranged separately under a predetermined portion of the wiring pattern connected to the connection pad.

[c4] 4. A wiring substrate according to claim 1 or 2, wherein the wiring substrate has a plurality of connection pads, a plurality of via holes associated with said plurality of connection pads are arranged in a state that a dummy via hole and normal via holes are arranged mixedly, and a normal via hole is arranged separately under a predetermined portion of the wiring pattern connected to the connection pad, in the wiring pattern in which the dummy via hole is arranged under the connection pad or the wiring pattern.

[c5] 5. A wiring substrate according to claim 3, wherein the normal via hole is arranged in a position that is away from the connection pad in excess of 200 μm.

[c6] 6. A wiring substrate according to claim 3, wherein a via post filled in the dummy via hole is formed between an upper surface of the via post and a lower surface of the connection pad or the wiring pattern via the insulating film.

[c7] 7. A wiring substrate according to claim 1 or 2, wherein the wiring substrate has a plurality of connection pads

corresponding to a plurality of bumps of the electronic parts, and a plurality of via holes associated with the plurality of connection pads, and
a diameter of the via holes formed in portions corresponding to both end portions of the electronic parts is set larger than a diameter of the via hole formed in a portion corresponding to a center portion of the electronic parts, in an oscillation direction of an ultrasonic wave applied when the electronic parts is packaged onto the wiring substrate by the ultrasonic flip-chip packaging.

[c8] 8. A wiring substrate according to claim 1 or 2, wherein the insulating film on the wiring substrate is made of resin.

[c9] 9. An electronic parts packaging structure comprising:
the wiring substrate set forth in Claim 1; and
the electronic parts whose bump is bonded to the connection pad of the wiring substrate by the ultrasonic flip-chip packaging.

[c10] 10. An electronic parts packaging structure according to claim 9, wherein the bump of the electronic parts is made of gold, and at least a surface layer portion of the connection pad of the wiring substrate is made of gold.